MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2016/2017

DCS5158 – COMPUTER ARCHITECTURE

(DIT Students Only)

26 MAY 2017
3:00 p.m. – 5:00 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENT:

1. This question paper consists of **6** pages with **2** sections.
2. Answer **ALL** questions.
3. For **Section A**, shade your answers on the OMR sheet provided.
4. For **Section B**, write your answers in the answer booklet provided.

SECTION A: MULTIPLE CHOICE QUESTIONS (MCQ) (20 Marks)

Instruction: *Answer **ALL** the questions in this section and shade your answers on the OMR sheet provided.*

1. According to Moore's Law, the number of transistors that can be implemented on a single chip will be _____every year and it is predicted that this pace would continue in future.
   A. decreased
   B. static
   C. doubled
   D. normalized

2. Which of the following is a high-level programming language that been use in Second Generation Computers?
   A. C.
   B. Java.
   C. Fortran.
   D. Pascal.

3. In a fetch cycle, the _____ interprets instruction and performs the required action.
   A. accumulator
   B. processor
   C. program counter
   D. instruction register

4. What is -43 in signed magnitude format with 8-bit representation?
   A. 10101011_2
   B. 10101010_2
   C. 11101011_2
   D. 10111011_2

5. What is the value of 2000_{10} in octal representation?
   A. 2347_8
   B. 3720_8
   C. 2730_8
   D. 2473_8

6. Opcodes are represented by abbreviations called _____.
   A. register
   B. mnemonics
   C. accumulator
   D. stack

Continued...

7. _____ provide computational capabilities for processing numeric data.
   A. Branch instructions
   B. Memory instructions
   C. I/O instructions
   D. Arithmetic instructions

8. Which of the following is **NOT** type of numerical data that is common in computers?
   A. Binary floating point.
   B. Binary integer.
   C. Fraction.
   D. Decimal.

9. Which of the following is **TRUE** about Immediate Addressing Mode?
   I. Simplest form of addressing
   II. Operand = Y
   III. The left most bit of the operand field is used as a sign bit
   IV. The size of number is restricted to the size of the address field

   A. I and II.
   B. I, II and IV.
   C. I, III and IV.
   D. All of the above.

10. In Indirect Addressing mode, how many references will be required to fetch the operand?
   A. One, for address only.
   B. Two, for address and value.
   C. Three, for address, value and operation.
   D. Four, for address, operation, value and result.

11. _____ is a memory chip on which data can be written only once. The writing process is performed electrically and may be performed by a supplier or customer later than the original chip fabrication.
   A. Random Access Memory (RAM)
   B. Erasable programmable read-only memory (EPROM)
   C. Programmable ROM (PROM)
   D. Read Only Memory

12. Which of the following refers to magnetic-surface memory in the data storage?
   A. Retaining data even if there is a break in the power supply.
   B. Cannot be altered, except by destroying the storage unit.
   C. Data will be lost once the power supply is off.
   D. All of above.

Continued...

13. Using the multiple disk, the transfer rate can be improved by_____ data and thus increase speed and performance.
    A. mirroring
    B. stripping
    C. parallel access
    D. independent access

14. The width of the_____ is the main factor to determine overall system performance in the processor.
    A. address bus
    B. bus lines
    C. data lines
    D. data bus

15. Referring to the figure below, which of the bus lines receive the request and transfer data to the other module?

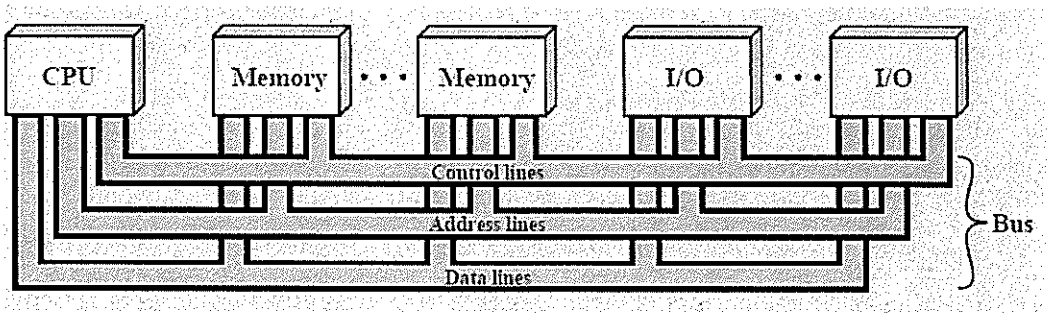

Figure 1

    A. Control and address lines.
    B. Control and data lines.
    C. Bus and data lines.
    D. Address and bus lines.

16. _____ is a technique where the processor issues a command to I/O and continues to execute the other instruction. The current instruction will be execute until finished and the previous instruction will continue when the current instruction done executed.
    A. Programmed I/O
    B. Interrupt handler
    C. Interrupt-driven I/O
    D. Direct Memory Access (DMA)

17. Which technique is used to identify request from the devices?
    A. Bus arbitration.
    B. Software polling.
    C. Daisy chain.
    D. Multiple interrupt lines.

Continued...

18. Which of the following is **FALSE** about the principle I/O techniques?
    A. Programmed I/O.
    B. Interrupt Driven I/O.
    C. Interrupt Handler.
    D. Direct Memory Access.

19. Which of the following is the **BEST** situation as illustrated in Figure 2?

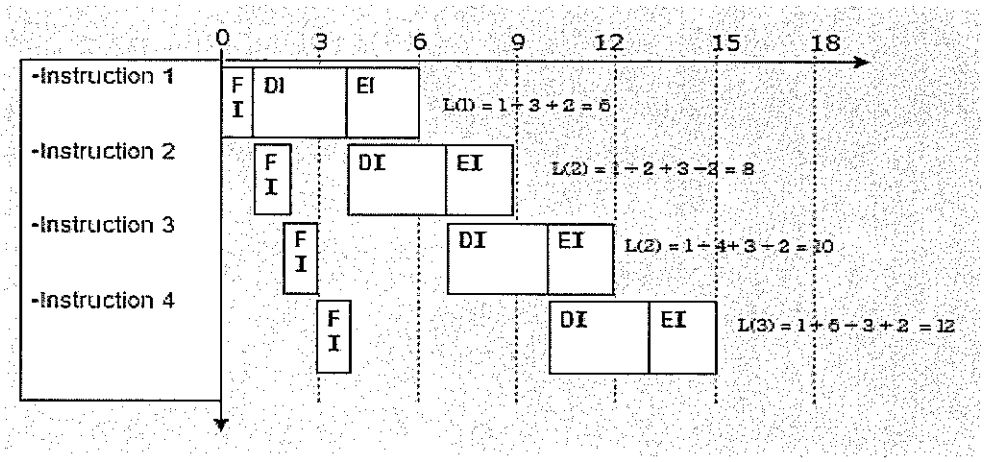

Figure 2

    A. Correct timing diagram.
    B. Latencies not constant.
    C. Overlaps timing diagram.
    D. Instruction not constant.

20. Which of the following is **TRUE** about the stages in the pipelining process?
    A. FI, DI, CO, FO, EI, WO
    B. FI, EI, WE, FE, CI
    C. FI, DI, CO, FI, EI, WO
    D. FI, DI, EI, FO, WO

Continued...

SECTION B: STRUCTURED QUESTIONS (80 Marks)

Instruction: *Answer ALL the questions in this section and write your answers in the answer booklet provided.*

QUESTION 1 (20 Marks)

a) Give the definition of computer architecture and computer organisation. Differentiate between computer organisation and computer architecture by using an analogy. (6 Marks)

b) Calculate $40_{10} - 72_{10}$ by using two's complement with 8-bit binary representation. (7 Marks)

c) Perform the following conversions. Show all the necessary steps.

i. Convert 184.59375_{10} (decimal) to a normalised binary value. (2 Marks)
ii. Convert $7F3.0E_{16}$ to its decimal equivalent. (2 Marks)
iii. Convert $EC8_{16}$ to its octal equivalent. (3 Marks)

QUESTION 2 (20 Marks)

a) Given the following Zero-address machine instructions:

Zero-Address
PUSH N
PUSH E
PUSH K
PUSH J
MUL
SUB
ADD
PUSH W
PUSH P
PUSH E
SUB
MUL
DIV
POP Y

i. State the expression of program execution. (1 Mark)
ii. Based on the expression in (i), write the following machine instructions:
- One-address (2.5 Marks)
- Two-address (2.5 Marks)

iii. Draw the stack diagrams that illustrate the program execution. (4 Marks)

Continued...

b) A computer system has a memory architecture made up of main memory of 4GB and cache of 8192KB. In order to perform an efficient mapping function, the main memory is arranged in blocks of 1024 bytes.

Draw the address structures for different mapping functions as stated below. Indicate the fields and the number of bits required for each field.

i. Direct Mapping (3.5 Marks)
ii. Associative Mapping (3 Marks)
iii. Eight-Way Set Associative Mapping (3.5 Marks)

QUESTION 3 (20 Marks)

a) Describe **FOUR (4)** procedures and components of a bus system that are important to run the data and to connect devices to each other. (8 Marks)

b) State **THREE (3)** differences between Address Bus and Control Bus. (6 Marks)

c) An external device connected to an I/O module is often referred to as a peripheral device or, simply, a peripheral. List and briefly explain **THREE (3)** categories of external devices with example. (6 Marks)

QUESTION 4 (20 Marks)

a) Draw a timing diagram for **SEVEN (7)** instructions where each instruction has **SEVEN (7)** stages (FI, DI, D2, CO, FO, EI and WO) with delays of 6, 2, 3, 5, 4, 8 and 3 seconds for each stage respectively. (6 Marks)

b) Based on (a), calculate the total processing time, speedup and throughput for the implementation of pipelining and non-pipelining.

(10 Marks)

(Note: You may refer to the given formula and write an appropriate answer]

$T_k = sum_{i=1}^{k} t_i + (n-1).\max_{i=1}^{k}\{t_i\}$	$T_o = \sum_{i=1}^{k} t_i$ n.
$T_k = (k + (n-1)]t$	$T_0 = nkt$

c) One of the most visible forms of evolution associated with computers is that of programming languages. State and explain **FOUR (4)** characteristics from the instruction execution process. (4 Marks)

End of Page.